Claim Rejections - 35 USC § 102

During the November 16, 1999 telephone interview, the Examiner indicated that claims 10, 31 and 33 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Larson et al. (U.S. Patent No. 5,793,386). In response, the Applicant has canceled claim 10, and amended claims 31 and 33. To aid in clarifying the manners in which such amendments serve to differentiate the Applicant's invention over Larson et al., a brief overview of Larson et al. and the Applicant's invention as set forth by amended claims 31 and 33 is provided.

Larson et al. disclose a graphics system in which a graphics controller receives a display list from a host processor, where the display list include only those values necessary for rendering a graphics primitive. The graphics controller includes a register file for into which the display list values are loaded or stored.

As stated beginning at column 5, line 66, "to load the display list values into the appropriate registers in the register file, each value in the display list has an associated address corresponding to a register in the register file." Larson et al. immediately thereafter state that a prefetch unit and an execution unit store any given display list value in a register corresponding to the register file address associated with the display list value. Larson et al. offer no further teachings or suggestions directed toward any manner of storing display list values in the register file.

Claim 31 as amended recites the following:

31. (Amended) A graphics system for storing display list values in a register file, wherein the display list is shortened to enable fast processing time while maintaining the quality of information contained in the display list, the graphics system comprising:

a register file, for storing at least one set of display list values, the register file comprising a plurality of registers;

a load instruction unit, for storing an instruction having an opcode portion that specifies a rendering operation, and a write-enable portion that spans a plurality of bits, wherein a first bit corresponds to a target starting register file address and subsequent bits sequentially correspond to register file addresses that follow the target starting register file address;

a shifter coupled to receive the write-enable portion, wherein the shifter sequentially performs single-bit shifts upon the contents of the write-enable portion; and

a rendering parameter storage controller coupled to the shifter and the register file, wherein the rendering parameter storage controller sequentially steps through register file addresses as write-enable portion bits are considered by the shifter, and stores a display list value in the register file in response to a write-enable portion bit under consideration by the shifter having a predetermined value.

Thus, claim 31 as amended includes a load instruction unit that stores an instruction. The instruction includes a write-enable portion spanning multiple bits. A first bit within the write-enable portion corresponds to a target starting register file address. Bits that follow the first bit sequentially correspond to register file addresses that follow the target starting register file address.

Claim 31 also specifies a shifter that is coupled to receive the write enable portion. The shifter sequentially performs single-bit shifts upon the contents of the write-enable

portion. Claim 31 additionally specifies a rendering parameter storage controller that sequentially steps through register file addresses as the shifter considers each write-enable portion bit. The rendering parameter storage controller stores a display list value in the register file when a write-enable portion bit being considered by the shifter has a predetermined value, for example, binary 1.

To summarize, claim 31 specifies a shifter that is coupled to receive a set of write-enable portion bits that comprise a portion of a rendering instruction. The write-enable portion bits sequentially correspond to register file addresses. The shifter performs single-bit shifts upon the set of write enable portion bits. A rendering parameter storage controller steps through register file addresses. When a write-enable portion bit that the shifter is considering has a predetermined value, the rendering parameter storage controller stores a display list value in the register file.

Larson et al. fail to disclose or suggest any type of shifter that serves as any type of element within an apparatus or means for storing display list values in a register file. Larson et al. also fail to disclose a rendering instruction that includes a write-enable portion, and further fail to disclose a rendering parameter storage controller responsive to bit values within the write-enable portion as such bit values are considered on a single-bit basis by the shifter. The Applicant respectfully submits that claim 31 as amended is patentably distinct over Larson et al., and request that the Examiner now withdraw the rejection of claim 31 under 35 U.S.C. § 102(e).

Claim 33 as amended recites the following:

33. (Amended) In a computer system having a graphics controller, a method for storing display list values in a register file comprising a plurality of addressable registers, wherein the display list is shortened to enable fast processing time while maintaining the quality of information contained in the display list, each display list value corresponding to a graphics primitive, the method comprising the steps of:

retrieving an instruction that includes an opcode portion and a write-enable portion, the opcode portion specifying a rendering operation, the write-enable portion spanning a plurality of bits, wherein a first bit corresponds to a target starting register file address, and subsequent bits sequentially correspond to register file addresses that follow the target starting register file address;

sequentially examining each bit within the write-enable portion; and

storing a display list value in the register file in response to a write-enable portion bit under examination having a predetermined value.

As per the detailed description in Larson et al. beginning at column 5, line 66, Larson et. al. disclose a technique for storing display list values in a register file in which each display list value has an associated address corresponding to a particular register in the register file. Each value included in the display list is stored at its corresponding register file address. Register file addresses not associated with the values included in the display list are not considered.

Claim 33 as amended recites the step of retrieving an instruction that includes a write-enable portion spanning multiple bits. A first bit within the write-enable portion corresponds to a target starting register file address, and subsequent write-enable portion bits sequentially

correspond to subsequent register file addresses. Amended claim 33 also recites the steps of sequentially examining each write-enable portion bit, and storing a display list value in the register file when a write-enable portion bit under examination has a predetermined value.

Larson et al. fail to disclose or suggest a rendering instruction that includes a write-enable portion as claimed. As a result, Larson et al. fail to disclose the steps of retrieving such a rendering instruction; sequentially examining each bit within the retrieved instruction's write-enable portion; and storing a display list value in a register file when a write-enable portion bit under examination has a predetermined value, for example, binary 1. The Applicant respectfully submits that claim 33 as amended is patentably distinct over Larson et al, and requests that the Examiner withdraw the rejection of claim 33 under 35 U.S.C. § 102(e).

Claims 31 through 34 are presently under consideration in this case. Claim 32 is dependent upon claim 31, and claim 34 is dependent upon claim 32. In view of the foregoing, the Applicant respectfully submits that claims 31-34 are patentably distinct over the cited art, and in condition for allowance. Reconsideration and prompt favorable action are therefore solicited.

Respectfully submitted,
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